What is claimed is:

1. A synchronous semiconductor device supporting at least two kinds of bit configuration modes, the synchronous semiconductor device comprising:

a first data bus which is used to transmit data in a first bit configuration mode and is not used to transmit data in a configuration mode other than the first bit configuration mode; and

a second data bus which is used to transmit data in the first bit configuration mode and a second configuration mode, is not used to transmit data in a configuration mode other than the first bit configuration mode and the second configuration mode, and is arranged to be parallel with the first data bus,

wherein the first data bus and the second data bus are arranged alternately.

2. The synchronous semiconductor device of claim 1, wherein the synchronous semiconductor device further comprises a third data bus which is used to transmit data in the first bit configuration mode, the second bit configuration mode, and a third bit configuration mode and is arranged to be parallel with the first data bus and the second data bus, wherein the third data bus is arranged crosswise to the first data bus and the second data bus.

3. The synchronous semiconductor device of claim 2, wherein the third bit configuration is Xn (n denotes a natural number more than 2), the second bit configuration is X2n, and the first bit configuration is X4n.

4. The synchronous semiconductor device of claim 2, wherein the first data bus is electrically connected to a supply voltage in the second bit configuration mode and the third bit configuration mode, and the second data bus is electrically connected to a supply voltage in the third bit configuration mode.

5. The synchronous semiconductor device of claim 4, wherein the supply voltage is a ground voltage.

6. The synchronous semiconductor device of claim 2, wherein the first data bus, the second data bus, and the third data bus are arranged between a bit line sense amplifier and an output buffer or between the bit line sense amplifier and an input buffer.

7. A synchronous semiconductor device which supports both a single data rate mode and a double data rate mode, the synchronous semiconductor device comprising:

a first data bus which is used to transmit data in the double data rate mode and is not used to transmit data in the single data rate mode; and

a second data bus which is used to transmit data in the single data rate mode and in the double data rate mode and is arranged to be parallel with the first data bus,

wherein the first data bus and the second data bus are arranged alternately.

8. The synchronous semiconductor device of claim 7, wherein the first data bus is electrically connected to a supply voltage or a ground voltage in the single data rate mode.

9. The synchronous semiconductor device of claim 7, wherein the first data bus and the second data bus are arranged between a bit line sense amplifier and an output buffer or between the bit line sense amplifier and an input buffer.

10. A method of shielding data buses in a synchronous semiconductor device which supports at least modes including a first mode and a second mode and uses a various number of data buses according to the mode, the method comprising:

classifying the data bus that is used to transmit data only in the first mode as a first data bus and classifying the data bus that is used to transmit data only in the second mode as a second data bus;

arranging the first data bus and the second data bus alternately; and

electrically connecting the first data bus to a supply voltage or a ground voltage in the second mode.

11. The method of claim 10, wherein the first mode is a double data rate mode, and the second mode is a single data rate mode.

12. The method of claim 10, wherein the first mode is a first bit configuration mode, and the second mode is a second configuration mode.